METHOD FOR PLANARIZING A WORK PIECE

TECHNICAL FIELD

[0001] The present invention generally relates to a method for planarizing a work piece, and more particularly relates to a method for planarizing a work piece such as a semiconductor wafer having a metal layer such as a copper containing metal layer on a surface thereof.

BACKGROUND

[0002] The production of integrated circuits begins with the creation of high-quality semiconductor wafers. During the wafer fabrication process, the wafers may undergo multiple dielectric and conductor deposition processes followed by the masking and etching of the deposited layers. Some of these steps relate to metallization, which generally refers to the materials, methods and processes of wiring together or interconnecting the component parts of an integrated circuit located on or overlying the surface of the wafer. Typically, the "wiring" of an integrated circuit involves etching trenches and "vias" in a planar dielectric (insulator) layer and filling the trenches and vias with a conductive material, typically a metal.

[0003] In the past, aluminum was used extensively as a metallization material in semiconductor fabrication due to ease with which aluminum could be applied and patterned and due to the leakage and adhesion problems experienced with the use of gold. Other metallization materials have included such materials as Ni, Ta, Ti, W, Ag, Cu/Al, TaN, TiN, CoWP, NiP and CoP, alone or in various combinations.

[0004] Recently, techniques have been developed which utilize copper to form conductive contacts and interconnects because copper is less susceptible to electromigration and exhibits a lower resistivity than aluminum. Since copper does not readily form volatile or soluble compounds, the patterned etching of copper is difficult, and the copper conductive contacts and interconnects are therefore often formed using a damascene process. In accordance with the damascene process, the copper conductive contacts and interconnects are usually formed by creating a via within an insulating material, depositing a barrier layer

onto the surface of the insulating material and into the via, depositing a seed layer of copper onto the barrier layer, and electrodepositing a copper layer onto the seed layer to fill the via. The excess copper and the barrier layer overlying the insulating material are then removed, for example by a process of chemical mechanical planarization or chemical mechanical polishing, each of which will hereafter be referred to as chemical mechanical planarization or CMP.

[0005] As the size of integrated circuit components continues to decrease and the density of microstructures on integrated circuits increases, the feature sizes found on the integrated circuit can vary widely from, for example, less than 100 nanometers (nm) to more than 1 micrometer (μm). Such features are generally spaced apart by otherwise substantially planar field regions. Filling the wide variety of features, especially the wide features, is difficult. To fill such wide features with a metal, it is often necessary to deposit relatively thick layers of the metal, typically 700 nm and greater, over the field regions of the wafer. A subsequent planarization process then is required to remove the thick excess deposited metal layers, to electrically isolate the metal in spaced apart features, and to level the surface for subsequent steps in the integrated circuit manufacturing process. Planarization of the thick metal layers by CMP is usually accomplished in a "soft landing CMP process" that involves several steps with each of the steps carried out on a different platen. First, the bulk of the excess metal is removed in a rapid removal process that uses a hard polishing pad attached to a polishing platen and employs a high pressure exerted between the wafer surface and the pad. The high pressure and the hard pad effect a rapid removal rate of the metal, but if continued to the completion of the metal removal, would result in damage to the underlying insulator, especially if that insulator is a low-k dielectric material. The hard pad also is effective for achieving a planar surface free from "dishing" of the metal in the vicinity of large features. In a second step, the final portion of the excess metal is removed using a hard polishing pad attached to a second platen but with a lower pressure exerted between the wafer surface and the polishing pad. The lower pressure is used to minimize dishing and erosion. A third step using yet another pad on another platen may then be required to remove the barrier layer overlying the field regions of the insulator. A final buff step may also be required to remove a damaged upper layer of the insulator, to remove contaminants, and to clean the resulting polished surface of the metal and the exposed insulator. Deposition of such thick layers of metal followed by a multi-step planarization process to subsequently remove the thick excess metal layer increases the costs of the planarization process and decreases throughput.

[0006] Accordingly, a need exists for an improved method for planarizing a work piece, and especially for planarizing a work piece having a deposited metal layer on a surface thereof. In addition, there is a need for a method for planarizing a semiconductor wafer having a deposited copper layer thereon. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and the foregoing technical field and background.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and wherein

[0008] FIGS. 1-3 illustrate, in cross section, steps in the deposition and planarization of a metal layer on a work piece in accordance with an embodiment of the invention;

[0009] FIG. 4 illustrates schematically, in cross section, apparatus in which a layer of metal can be deposited on a work piece in accordance with an embodiment of the invention;

[0010] FIG. 5 illustrates schematically, in cross section, apparatus in which a work piece can be planarized in accordance with an embodiment of the invention; and

[0011] FIGS. 6 and 7 schematically illustrate alternative embodiments for controlling slurry composition in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

[0012] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, or the following detailed description.

[0013] The invention disclosed and claimed herein is applicable to the planarization of a surface of a variety of work pieces, but will be described and illustrated with reference to

only a single illustrative work piece, namely a semiconductor wafer having a layer of copper deposited thereon. Although the invention is illustrated with reference to its application only to one particular work piece and to one particular metal deposited on that work piece, it is not intended that the invention be limited to that particular application.

[0014] FIGS. 1-3 illustrate process steps in accordance with an embodiment of the invention. FIG 1 illustrates, in cross section, a portion of a partially processed semiconductor wafer 10. Wafer 10 includes a semiconductor substrate 12 which can be, for example, a silicon substrate. Overlying substrate 12 is a layer 14 of insulating material. Although shown as only a single insulating layer, the layer of insulating material may be a single layer of insulating material or may be composed of a plurality of layers of insulating material, not all of which are necessarily the same material. The layer of insulating material may be or may include, for example, silicon dioxide, silicon nitride, or any of the other insulating materials commonly used in the fabrication of semiconductor devices. In accordance with one embodiment of the invention layer 14 may include a layer of low-k dielectric material such as those formed by spin on deposition from, for example, an organic source material comprising polyimide, silicon sesquioxane, siloxane, or the like. By low-k dielectric material is meant a material having a dielectric constant less than about 3.9. Various layers of conductive material such as conductors 16 and 18 may be embedded in layer 14. Conductors 16 and 18 can be, for example a portion of a previously deposited and patterned layer of metal, doped polycrystalline silicon, metal silicide, or the like. Features 20 and 22 are formed in the surface of layer 14. As used herein, a feature is any sub-surface element, character or surface such as, but not limited to, a via or trench formed within the layer of insulating material. As illustrated, features 20 and 22 may be vias or trenches allowing subsequent electrical contact to be made to conductors 16 and 18. The features can be formed by conventional photolithographic and etching techniques. The surface of layer 14 surrounding features 20 and 22 is called the field region 24. Field region 24 is any adjacent element, character or surface that is elevated with respect to the features. The field region is generally, but not necessarily, substantially planar in contrast to the features. Features formed during the processing of a semiconductor device can be of varying sizes. As illustrated, feature 20 is wider in extent than is feature 22. For illustrative purposes only, feature 20 can be considered to have a width of 1-2 μm or even larger while feature 22 can be considered to have a minimum feature size of less than 100 nm.

[0015] FIG. 2 illustrate, again in cross section, continuing steps in accordance with an embodiment of the invention. A barrier layer 25 is formed overlying the surface of layer 14 and extending into features 20 and 22. Barrier layer 25 can be formed by physical vapor deposition or chemical vapor deposition to a thickness of, for example, about 25 nm or less. The barrier layer can be formed of tantalum, tantalum nitride, or other suitable barrier material capable of retarding the migration into insulating layer 14 of copper from a subsequently formed copper layer. A seed layer 26 of copper is next formed overlying the barrier layer. The seed layer can be formed by physical vapor deposition, chemical vapor deposition, or electroless deposition. Following the formation of seed layer 26, a thick layer of copper 28 or 30 is deposited overlying the seed layer. The copper layer is deposited to a sufficient thickness that all of the features are completely filled with copper. In accordance with the prior art conventional method, a copper layer 28, the extent of which is indicated by dashed line 32, was deposited by an electroplating process. To completely fill all features, and especially large features such as feature 20, the layer was deposited to a thickness of 0.7-1.3 μm. The thick layer overlying the field regions, referred to as an "overburden," must subsequently be removed by a multi-step planarization process. Both the deposition of such a thick layer and the subsequent multi-step planarization process are time consuming and costly.

[0016] In contrast to the prior art conventional method, in accordance with an embodiment of the invention, a copper layer 30 having a substantially planar upper surface 34 is deposited overlying the seed layer by an electrodeposition process such as that disclosed in the copending, commonly assigned application filed February 27, 2003 and identified by attorney docket number 004.0029, the disclosure of which is herein incorporated in its entirety by reference. As used herein the term "substantially planar surface" shall mean a surface having no step height greater than about 100 nm and as used hereinafter, the term "electrodeposition" includes both the processes of electroplating and electrochemical mechanical deposition, also known as planar deposition. Electroplating typically involves conventional metal deposition using an electrolyte solution containing a metal, an anode, and a cathode. Electrochemical mechanical deposition uses a dedicated apparatus that selectively deposits the metal on the work piece by a process that combines electroplating with a mechanical aspect to obtain a planar metal surface of a desired thickness.

[0017] The following example illustrates a method, in accordance with one embodiment of the invention, for performing substantially planar deposition of a copper layer on

semiconductor wafer 10. The copper layer can be deposited in a variety of different deposition apparatuses that are well known in the industry such as, for example, an electrochemical mechanical deposition apparatus 60 schematically illustrated in FIG. 4. To effect substantially planar electrochemical deposition, apparatus 60 utilizes a contact surface 62 supported by a platen 64. The semiconductor wafer having a barrier layer and seed layer as previously described is urged against contact surface 62 by a wafer carrier assembly 68. Platen 64 may be fabricated from a conductive material, such as copper, tantalum, gold or platinum, or may be formed of an inexpensive material, such as aluminum or titanium, and coated with a conductive material. Using a power source 70, the apparatus applies a negative potential to the semiconductor wafer through a cathode contact 72, and a positive potential to the platen 64, which acts as an anode. Cathode contact 72 may comprise one or more contacts and may contact the semiconductor wafer by a variety of known methods. For example, contact 72 may be insulated from and disposed within platen 64 to contact the face of the semiconductor wafer or may be remote from platen 64 and may contact the face of the semiconductor wafer at its peripheral edge.

[0018] Platen 64 may be connected to a driver or motor assembly (not shown) that is operative to rotate platen 64 and contact surface 62 about a vertical axis. It will be appreciated by those of skill in the art, however, that the driver or motor assembly may be operative to move platen 64 and contact surface 62 in an orbital, linear or oscillatory pattern or any combination thereof. Similarly, wafer carrier 68 may be connected to a driver or motor assembly (not shown) that is operative to rotate wafer carrier 68 and the semiconductor wafer about a vertical axis 76 or to move wafer carrier 68 and the semiconductor wafer in an orbital, linear or oscillator pattern or any combination thereof.

[0019] Platen 64 may have one or more channels 74 for the transportation of a plating composition to contact surface 62 from a manifold apparatus (not shown) or any suitable distribution system. Alternatively, it will be appreciated that the plating composition may be deposited directly on or through contact surface 62 by a conduit or any suitable application mechanism. As a further alternative, the platen and contact surface may be immersed in the plating solution which is contained within a receptacle or container that partially surrounds the platen.

[0020] The method for performing substantially planar deposition of a metal on a semiconductor wafer, in accordance with one exemplary embodiment of the invention,

comprises selecting a deposition temperature, that is, the predominant or average temperature at which the deposition process will be conducted. An electrodeposition composition is formulated comprising a metal salt, a suppressor, an accelerator, and an electrolyte with the suppressor chosen so that it has a cloud point that is no greater than the selected deposition temperature. In accordance with a particular embodiment of the invention, the suppressor is selected so that the cloud point matches the deposition temperature. If the cloud point is greater than the deposition temperature, an anion may be added to the composition to lower the cloud point to a temperature no greater than the electrodeposition temperature. For example, for a deposition temperature of 21°C, the composition may comprise 67 g/L $CuSO_4 \bullet 5H_2O$, 180 g/L H_2SO_4, 10 ml/L of 2 % Pluronic® 31R1 (available from BASF Corporation of Mount Olive, New Jersey), 7 ml/L of 0.1% of the sodium salt of 3-mercaptopropane sulfonic acid and 50 ppm bromide. The components of the composition may be combined in any suitable order by any convenient method of mixing, such as, for example, by rapidly stirring with a mechanical stirrer or by agitating with a mechanical agitator.

[0021] Next, metal is electrodeposited onto the semiconductor wafer from the electrochemical deposition composition. The electrodeposition occurs at the selected deposition temperature. Wafer carrier 68 urges the semiconductor wafer against contact surface 62 such that the semiconductor wafer engages contact surface 62 at a desired pressure. Preferably, wafer carrier 68 applies a uniform and constant pressure of approximately 1 pound per square inch (psi) or less, although it may be appreciated that any suitable pressure that promotes substantially planar deposition may be used. During the deposition process, the electrodeposition composition is delivered to the surface of contact surface 62 through channels 74. An electric potential is also applied to create a circuit between platen 64, the electrodeposition composition and the semiconductor wafer. The power source 70 may apply a constant current or voltage to the apparatus or, alternatively, the current or voltage could be modulated to apply different currents or voltages at predetermined times in the process or to modulate between a predetermined current or voltage and no current or no voltage. Wafer carrier 68 and the semiconductor wafer may rotate about axis 76 while platen 64 and contact surface 62 move in a rotational, orbital or linear pattern. In addition, wafer carrier 68 and the semiconductor wafer may oscillate relative to contact surface 62. The electrodeposition process continues for a predetermined

amount of time or until an endpoint detection apparatus indicates that a desired deposition thickness has been achieved.

[0022] Following the deposition of copper layer 30 having a thin overburden and a substantially planar upper surface 34, the excess copper and barrier layer overlying the field regions of layer 14 of dielectric material are removed by a chemical mechanical planarization (CMP) process to achieve the desired structure illustrated in FIG. 3. The copper and barrier layer filling features 20 and 22 are electrically isolated from each other by the planarization process and the remaining copper has a substantially planar upper surface 36. Both upper surface 36 of the copper and the substantially planar upper surface of layer 14 of dielectric material are substantially free from scratches and other defects.

[0023] In accordance with one embodiment of the invention, the planarization of copper layer 30 can be accomplished in a CMP apparatus such as a Momentum CMP apparatus available from Novellus Systems Inc., CMP Division, of Chandler, Arizona. A representative CMP apparatus 80 in which the planarization can be carried out is schematically illustrated, in cross section, in FIG. 5. This apparatus is merely exemplary of CMP apparatus that can be employed in carrying out a CMP process in accordance with various embodiments of the invention. CMP apparatus 80 includes a carrier head 82 for controllably pressing a semiconductor wafer such as semiconductor wafer 10 having a substantially planar copper layer 30 on a front surface thereof against a polishing pad 86. Carrier head 82 includes a rigid casing having a cavity 88 on a lower surface. A flexible membrane 90 is stretched across the cavity and presses against the back surface of the semiconductor wafer. A wear ring 92 is attached to the rigid carrier head with a resilient attachment here illustrated by springs 94. The wear ring surrounds cavity 88 and serves to precondition the polishing pad and to contain the lateral movement of the semiconductor wafer, thus maintaining the semiconductor wafer in position on the underside of carrier head 82. Carrier head 82 is attached to a shaft 96 by means of which the correct downward pressure can be applied to the carrier head and hence between the semiconductor wafer and the polishing pad. Shaft 96 may also be used to impart a rotational motion to carrier head 82 to improve the uniformity of the polishing action. The polishing pad is mounted on a platen 98. In accordance with a preferred embodiment of the invention, polishing pad 86 is a soft polishing pad such as a Politex© pad available from Rodel, Inc. of Newark, Deleware. By "soft polishing pad" is meant a polishing pad having a hardness less than about 0.4 on the Shore D hardness scale. Polishing pad 86 is "soft" in contrast to "hard" polishing pads such

as the IC1000 polishing pad also available from Rodel, Inc. Although hard polishing pads have in the past been thought necessary to achieve a substantially planar surface when performing a CMP process on an electroplated copper layer, the present inventors have discovered that such hard polishing pads are not necessary to achieve the desired substantially planar surface when the copper layer to be polished and planarized initially has a substantially planar upper surface and does not have a thick overburden overlying the field regions of the dielectric layer.

[0024] As a specific exemplary illustration, consider a semiconductor wafer prepared in the manner described above and having a barrier layer of TaN having a thickness of about 25 nm, a seed layer of copper having a thickness of about 80 nm, and a copper overburden on the field regions of the dielectric material having a thickness of less than about 300 nm and preferably less than about 200 nm. Such a semiconductor wafer can be planarized on a Momentum CMP apparatus using a soft polishing pad such as a Politex© polishing pad, a polishing pressure of about 0.5-2.5 pounds per square inch (psi) and preferably a pressure of about 1 psi, a wafer rotation of about 600 revolutions per minute and an orbital platen motion with an orbit radius of about 1.25 inches. The planarization process proceeds for about 100 seconds and then the wafer is transferred to a buff station or directly to a cleaning station. The complete planarization process is carried out on the single polishing pad, preferably a soft polishing pad affixed to a single platen to remove the excess copper overburden and the barrier layer overlying the field regions of the insulating layer. In accordance with one embodiment of the invention the slurry preferably is selected to have substantially the same selectivity to copper as it does to the barrier layer. That is, the removal rate of the copper and the removal rate of the barrier layer are substantially in the ratio of 1:1. For example, a slurry such as Hitachi T-805-H can be employed with the concentration of hydrogen peroxide oxidizing agent adjusted to about 0.5%. The planarization process can also be continued on the same soft polishing pad to planarize the field regions of the dielectric material. The use of a soft polishing pad and low pressures between the wafer surface and the polishing pad are especially advantageous in avoiding scratching or otherwise causing damage to the dielectric layer if the layer of dielectric material includes a low-k dielectric.

[0025] In accordance with a further embodiment of the invention, the planarization of copper layer 30 is carried out as above except that the slurry composition is adjusted during the process to first provide an enhanced copper removal rate and then a reduced and

controlled copper removal rate. For example, Hitachi T-805-H slurry can be employed with the hydrogen peroxide oxidizing agent adjusted to about 3% at the point of use to enhance the copper removal rate during the bulk copper removal step and then reduced to about 0.5% to achieve a selectivity of about 1:1 with the barrier material. During the bulk copper removal rate step the selectivity of the removal of copper with respect to the removal of the barrier layer can be greater than 1:1. The change in concentration of the oxidizing agent can be made based on time of polishing or based on end point detection in known manner. When the slurry composition is to be changed, the pad and associated apparatus can be flushed with water to purge the system of the first slurry composition. FIGS. 6 and 7 schematically illustrate two alternative embodiments of processing equipment 100 and 200 respectively, for controlling the slurry composition, each operative with CMP apparatus such as that illustrated in FIG. 5.

[0026] FIG 6 schematically illustrates processing equipment 100 for controlling the composition of slurry employed in accordance with an embodiment of the invention. Equipment 100 includes a polishing pad 86 mounted on a platen 98. Platen 98 is configured to provide a slurry distribution manifold 102. The slurry distribution manifold is in fluid communication with a plurality of slurry transport channels 104 through the upper surface of platen 98 and polishing pad 86. Two reservoirs 106 and 108 are provided for premixed slurry. Reservoir 106 contains a slurry having a high (for example, about 3%) concentration of oxidizing agent for the rapid removal of copper, and reservoir 108 contains a slurry having a low (for example, about 0.5%) concentration of oxidizing agent to achieve a selectivity of about 1:1 for copper:barrier layer. Reservoir 106 is coupled to manifold 102 through conduit 110. The flow of slurry from reservoir 106 to manifold 102 is controlled by a pump 112. Similarly, reservoir 108 is coupled to manifold 102 through conduit 114, and the flow of slurry from reservoir 108 to manifold 102 is controlled by a pump 116. Flow controllers or the like may also be coupled to pumps 112 and 116 to accurately control the flow of slurry. A water line 118 may also be coupled to manifold 102 to aid in purging the manifold, slurry transport channels, and polishing pad when a change is made from one slurry composition to the other slurry composition.

[0027] FIG 7 schematically illustrates processing equipment 200 for controlling the composition of slurry employed in accordance with a further embodiment of the invention. Equipment 200 includes a polishing pad 86 mounted on a platen 98. Platen 98 is configured to provide a slurry distribution manifold 202. The slurry distribution manifold is in fluid

communication with a plurality of slurry transport channels 204 through the upper surface of platen 98 and polishing pad 86. Reservoir 206 for slurry and reservoir 208 for an oxidizing agent such as hydrogen peroxide are coupled to the slurry distribution manifold through conduit 210 and flow controllers 212 and 214. Reservoir 206 can be filled with a CMP slurry such as Hitachi T-805-H. Flow controllers 212 and 214 control the flow of slurry and oxidizing agent, respectively, to premix the appropriate slurry composition prior to reaching the slurry distribution manifold. Upon reaching the end point of the bulk copper removal, flow controller 214 decreases the amount of oxidizing agent mixed with the slurry to achieve the desired 1:1 selectivity of copper:barrier layer. A water line 218 may also be coupled to manifold 202 to aid in purging the manifold, slurry transport channels, and polishing pad when a change is made from one slurry composition to the other slurry composition.

[0028] The resulting wafer is found to have a substantially planar upper surface. The remaining copper regions are planar and free from dishing. The field regions of the dielectric layer are substantially planar and substantially free from defects and scratches.

[0029] Although the exemplary CMP apparatus described above is of the type generally referred to as a front referenced apparatus, the method of the invention is also applicable to other types of CMP apparatus such as, for example, back referenced apparatus. In such an apparatus the planar removal of the copper layer and the underlying barrier layer are carried out on a single platen using a soft polishing pad and preferably a slurry having a copper:barrier selectivity of about 1:1. In accordance with yet another embodiment of the invention, the processes of planarized deposition and subsequent CMP can also be performed in a single continuous operation. That is, the apparatus for planarized deposition of a metal such as copper can also be used for the planarization of the resulting copper layer by switching from an electrochemical deposition composition applied to the polishing pad or contact surface to a polishing slurry applied to the polishing pad. The pressure of the semiconductor wafer against the polishing pad during the two operations can be adjusted to the appropriate pressure as described above.

[0030] In accordance with a further embodiment of the invention, following the planarization of the deposited copper layer by any of the above described processes, the surface of the planarized semiconductor wafer, including both the planarized copper regions filling the features in the dielectric material and the field regions of the dielectric material

can be cleaned and buffed at a buffing station to complete the planarization of the field regions and to remove contaminants, CMP residue, residual damage, and the like from the surface of the wafer.

[0031] In accordance with an embodiment of the invention, the deposition apparatus as illustrated in FIG. 4 and the planarization apparatus illustrated in FIG. 5 or any of the variants thereof as described above can be can be combined as two elements of a multiple platen deposition and planarization apparatus. For example the deposition platen of FIG. 4 can be positioned in close proximity to the polishing platen of FIG. 5. The semiconductor wafer upon which the copper layer is to be deposited and planarized can be transferred or transported from a carrier head associated with and aligned with the deposition platen to a carrier head associated with and aligned with the polishing platen either manually or by a robot. Alternatively, the semiconductor wafer can be carried by a single carrier head that is positioned first with respect to the deposition platen and then with respect to the polishing platen. Such multi-platen apparatuses can also include a buff station for effecting the final buff and clean of the planarized wafer surface on a third platen.

[0032] While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the exemplary embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope of the invention as set forth in the appended claims and the legal equivalents thereof.